

Atty. Docket No.: NLMI.P133

PATENT

IN THE UNITED STATES PATENT OFFICE

In Re Patent Application of:

First Named Inventor: Srinivasan, Varadarajan

Application No.: 10/681,525

Filed: 10/8/2003

Title: CONTENT ADDRESSABLE MEMORY WITH
LATCHING SENSE AMPLIFIER

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450


Examiner: Not Yet Assigned

Art Unit: 2818

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450 on January 14, 2004

Charles E. Shemwell

(Name of Person Mailing Correspondence)

 Jan 14, 2004
Signature Date

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

Sir:

Enclosed is an Information Disclosure Citation Form PTO/SB/08A together with a copy of each reference cited therein. It is respectfully requested that the cited references be considered and that the enclosed copy of the Form PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant.

This Information Disclosure Statement is being submitted pursuant to 37 CFR 1.97(b). No fee is believed to be due.


Pursuant to 37 CFR 1.97(h), the submission of this Information Disclosure Statement is not to be construed as an admission that the information cited in this statement is material to patentability.

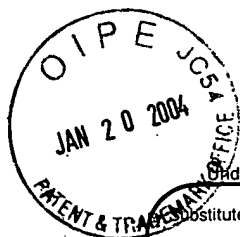
The Commissioner is hereby authorized to charge any fees which may be required in connection with this submission to Deposit Account No. 501914.

Respectfully submitted,

SHEMWELL GREGORY & COURTNEY LLP

Date January 14, 2004


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PTO/SB/08B (08-03)

Approved for use through 07/31/2006. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	10/681,525
		Filing Date	10/8/2003
		First Named Inventor	Srinivasan, V.
		Art Unit	2818
		Examiner Name	
Sheet 1	of 1	Attorney Docket Number	NLMI.P133

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SAKURAI, T. et al., "A Low Power 46ns 256k bit CMOS Static RAM with Dynamic Double Word Line," IEEE Journal of Solid State Circuits, Vol. SC-19, No.5, October 1984, pp.578-585	
		SOOD, L. et al., "A Fast 8ki x 8 CMOS SRAM With Internal Power Down Design Techniques," IEEE Journal of Solid State Circuits, Vol. SC-20, No. 5, October 1985, pp.941-950	
		MIYAJI, F. et al., "A 25-ns 4-Mbit CMOS SRAM with Dynamic Bit-Line Loads, IEEE Journal of Solid state Circuits," Vol. 24, No. 5, October 1989, pp.1213-1218	
		SASAKI, K. et al., "A 7-ns 140mW 1-Mb CMOS SRAM with Current Sense Amplifier," IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pp. 1511-1518	
		PRINCE, B., "Semiconductor Memories: A Handbook of Design, Manufacture and Application," 2nd Ed., John Wiley & Sons Ltd., West Sussex, England, 1995, pp. v-xvii, 401-404 and 4	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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